In re Patent Application of:
**ROCHE ET AL.**
Serial No.  **10/039,765**
Filing Date: **NOVEMBER 7, 2001**
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<u>REMARKS</u>

Applicants would like to thank the Examiner for the
thorough examination of the present application. In view of
the arguments presented in detail below, it is submitted that
all of the claims are patentable.

## I.   The Claimed Invention

The present invention is directed to a method of
transmitting data between two devices via a clock line and at
least one data line, the clock line being maintained by
default on a first logic value. As recited in independent
Claim 20, for example, the method includes providing each
device with the ability to tie the clock line to a potential
representing a second logic value opposite the first logic
value, and tying the clock line to the second logic value, via
the two devices, when data is transmitted. The method further
includes maintaining the tie to the clock line by the device
to which the data is sent while the device has not read the
data, and maintaining the data on the data line by the device
sending the data at least until an instant when the clock line
is released by the device to which the data is sent.

Independent Claim 32 is directed to a similar
method, independent Claims 44 and 46 are directed to related
data transmitting/receiving devices, independent Claim 48 is
directed to a related synchronous data transmission system,
and independent Claim 51 is directed to a related
communication interface circuit.

## II.   The Claims Are Patentable

The Examiner rejected independent Claims 20, 32, 44,

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46, 48, and 51 based upon the $I^2C$ Bus Specification, Version 2.1 (the "Specification"). The Examiner notes that an $I^2C$ bus includes a data line SDA and a clock line SCL. The Examiner points to FIG. 5 on page 9 of the specification and further to section 7.1 on page 10, which states that "[i]f a slave can't receive or transmit another complete byte of data until it has performed some other function, for example servicing an internal interrupt, it can hold the clock line SCL LOW to force the master into a wait state." The Examiner therefore contends that the Specification teaches all of the recitations of the above-noted independent claims.

It is respectfully submitted that the Examiner mischaracterizes the Specification.  A patentable distinction between the Specification and the claimed invention lies in that the claimed invention provides transmission of data when the clock signal is in the second logic value.  That is, when the clock signal is in a state different from the default state (first logic value) since this state can be controlled by both the master and the slave.  This advantageously allows the slave to control the duration of the transmission of each bit.

The Specification is based on an opposite concept. In page 11, chapter 8.1 of the Specification, second sentence, "data is only valid during the high period of the clock signal" which is the same as the default state.  This rule is confirmed by all the chronograms, as shown in FIGS. 9 and 10, for example.

This indication is perfectly clear and means that the transfer time of a bit is defined by the duration of the period when the clock signal is released (i.e., at a high

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level). Thus, the bit duration is controlled by the master
only since the high level of the clock signal is the default
value.

The handshake described in the Specification allows
the slave to "take its time" to compute the bit, since it can
control the instant when the next bit will be sent by tying
the clock signal to 0 after the precedent bit is received. But
the slave does not control the time allowed to read the bit,
i.e., the bit transmission time.

Thus the $I^2C$ data transmission method can be
summarized as follows:

Step 1) the master ties the clock signal to the low
states;

Step 2) the bit is positioned by the master when the
clock signal is low;

Step 3) the master releases the clock signal to
indicate to the slave that the bit is valid. However, if the
slave simultaneously forces the clock signal at a low state at
step 2), the master cannot release it and thus the bit is not
transmitted because data is only valid during the high period
of the clock signal. In this case the master waits until the
clock signal is released before starting counting the
transmission time; and

Step 4) the clock is high and the bit is transmitted
during a time lag under the control of the master.

Thus, even if the slave maintains the clock signal
in the low states, that does not enable it to extend the bit
transmission time (corresponding to the read time). The only
thing the slave can make by maintaining the clock signal in
the low state is to delay the sending of the next bit, as

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explained above.

On the contrary, with the claimed invention, a bit
is valid when the clock signal is in the low state.
Consequently, the invention makes it possible to keep the bit
valid during a period controlled by both the master and the
slave.  A distinction between the claimed invention and the $I^2C$
is due to the fact that the high state of the clock signal is
the default state and the default state cannot be controlled
by a handshake.

To summarize, with the invention, a bit is
transmitted (and read) when the clock signal is not in the
default state and both the slave and the master controls the
transmission time.  According to the Specification, a bit is
transmitted (and read) when the clock signal is in the default
state and the slave does not control the transmission time but
can only delay the transmission of the next bit.

It is submitted that the following is not disclosed
in the Specification because they are opposite to the rule in
the Specification according to which data is only valid during
the high period of the clock signal: maintaining the tie to
the clock line by the device to which the data is sent while
the device has not read the data; and maintaining the data on
the data line by the device sending the data at least until an
instant when the clock line is released by the device to which
the data is sent.

Accordingly, the Specification simply fails to teach
or fairly suggest all of the recitations of independent Claims
20, 32, 44, 46, 48, and 51. Thus, it is submitted that these
claims are patentable over the prior art. Their respective
dependent claims, which recite yet further distinguishing

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features, are also patentable over the prior art and require no further discussion herein.

### III. CONCLUSIONS

In view of the foregoing, it is submitted that all of the claims are patentable. Accordingly, a Notice of Allowance is respectfully requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

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### CERTIFICATE OF FACSIMILE TRANSMISSION

I HEREBY CERTIFY that the foregoing correspondence has been forwarded via facsimile number 571-273-8300 to the Commissioner for Patents on this _14_ day of August, 2006.

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